

What is claimed is:

Claims:

1     1. A vertical semiconductor device structure, comprising:  
2         a substrate defining a substantially horizontal plane;  
3         a gate electrode projecting vertically from said substrate;  
4         at least one semiconducting nanotube extending vertically through said gate  
5         electrode between opposite first and second ends;  
6         a gate dielectric electrically insulating said at least one semiconducting  
7         nanotube from said gate electrode;  
8         a source electrically coupled with said first end of said at least one  
9         semiconducting nanotube; and  
10         a drain electrically coupled with said second end of said at least one  
11         semiconducting nanotube.

1     2. The semiconductor device structure of claim 1 wherein said source is  
2         composed of a catalyst material effective for growing said at least one semiconducting  
3         nanotube.

1     3. The semiconducting device structure of claim 1 wherein said drain is  
2         composed of a catalyst material effective for growing said at least one semiconducting  
3         nanotube.

1     4. The semiconductor device structure of claim 1 further comprising:  
2         an insulating layer disposed between said drain and said gate electrode for  
3         electrically isolating said drain from said gate electrode.

1       5.     The semiconductor device structure of claim 1 further comprising:  
2              an insulating layer disposed between said source and said gate electrode for  
3              electrically isolating said source from said gate electrode.

1       6.     The semiconducting device structure of claim 1 wherein said at least one  
2              semiconducting nanotube is composed of arranged carbon atoms.

1       7.     The semiconducting device structure of claim 1 wherein said at least one  
2              semiconducting nanotube defines a channel region of a field effect transistor having a  
3              channel along which current flow is regulated by application of a control voltage to  
4              said gate electrode.

1       8.     The semiconducting device structure of claim 1 wherein said at least one  
2              semiconducting nanotube is oriented substantially perpendicular to said horizontal  
3              plane.

1       9.     The semiconducting device structure of claim 1 further comprising:  
2              a plurality of semiconducting nanotubes extending vertically through said gate  
3              electrode.

1       10.    The semiconducting device structure of claim 1 wherein said gate dielectric is  
2              disposed on said at least one semiconducting nanotube.

- 1      11.     A method of forming a semiconductor device structure comprising:  
2                forming a conductive pad on a substrate;  
3                growing at least one semiconducting nanotube extending substantially  
4                vertically from the conductive pad between a first end electrically coupled with the  
5                conductive pad and a second free end;  
6                electrically insulating the at least one semiconducting nanotube with a gate  
7                dielectric;  
8                forming a gate electrode electrically insulated from and overlying the  
9                conductive pad with the at least one semiconducting nanotube extending vertically  
10               through the gate electrode; and  
11               forming a contact electrically coupled with the second end of the at least one  
12               semiconducting nanotube and electrically insulated from the gate electrode.
  
- 1      12.     The method of claim 11 wherein electrically insulating the at least one  
2                semiconducting nanotube comprises:  
3                encasing the at least one semiconducting nanotube inside the gate dielectric.
  
- 1      13.     The method of claim 11 wherein forming the contact comprises:  
2                removing the gate dielectric from the free end of the at least one  
3                semiconducting nanotube; and  
4                providing a metal feature operating as said contact.
  
- 1      14.     The method of claim 13 further comprising:  
2                forming an insulating layer on the gate electrode; and  
3                recessing the insulating layer to expose the free end of the at least one  
4                semiconducting nanotube.

1       15.     The method of claim 11 wherein the at least one semiconducting nanotube is a  
2     carbon nanotube and the conductive pad is formed of a catalyst material suitable for  
3     growing carbon nanotubes, and growing the at least one semiconducting nanotube  
4     further comprises:

5                 exposing the conductive pad to a carbonaceous reactant under conditions  
6     effective to incorporate carbon atoms into the carbon nanotube with a semiconducting  
7     molecular structure.

1       16.     The method of claim 11 wherein growing the at least one semiconducting  
2     nanotube further comprises:

3                 growing the at least one semiconducting nanotube by a chemical vapor  
4     deposition technique.

1       17.     The method of claim 11 wherein the free end of the at least one  
2     semiconducting nanotube projects into a metal constituting the contact.

1       18.     The method of claim 11 wherein the at least one semiconducting nanotube is  
2     characterized by arranged carbon atoms.

1       19.     The method of claim 11 wherein the at least one semiconducting nanotube  
2     defines a channel region of a field effect transistor having a channel regulated by  
3     application of a control voltage to the gate electrode.

1       20.     The method of claim 11 wherein forming the gate electrode comprises:  
2                 applying an insulating layer on the conductive pad;  
3                 applying a conductive layer overlying the insulating layer; and  
4                 patterning the conductive layer to define the gate electrode.

- 1      21.     The method of claim 20 wherein forming the contact comprises:  
2                recessing the insulating layer to expose the free end of the at least one  
3        semiconducting nanotube.
  
- 1      22.     The method of claim 21 further comprising:  
2                removing the gate dielectric from the free end of the at least one  
3        semiconducting nanotube; and  
4                providing a metal feature operating as said contact.
  
- 1      23.     The method of claim 11 wherein said at least one semiconducting nanotube  
2        defines a channel region of a field effect transistor having a channel along which  
3        current flow is regulated by application of a control voltage to said gate electrode.
  
- 1      24.     The method of claim 11 further comprising:  
2                growing at least one conducting nanotube extending substantially vertically  
3        from the conductive pad; and  
4                destroying the at least one conducting nanotube before forming the gate  
5        electrode.

- 1      25.     A semiconductor device structure, comprising:
  - 2            a substrate defining a substantially horizontal plane;
  - 3            a conductive first plate disposed on said substrate,
  - 4            at least one nanotube projecting vertically from said first plate and electrically
  - 5            coupled with said first plate;
  - 6            a conductive second plate positioned vertically above said first plate; and
  - 7            a dielectric layer electrically isolating said second plate from said first plate
  - 8            and said at least one carbon nanotube.
  
- 1      26.     The semiconductor device structure of claim 25 wherein said at least one  
2        nanotube has a conducting molecular structure.
  
- 1      27.     The semiconductor device structure of claim 25 wherein said at least one  
2        nanotube has a semiconducting molecular structure.
  
- 1      28.     The semiconducting device structure of claim 25 wherein said dielectric layer  
2        defines a coating that encases said at least one nanotube.

1        29.     A method of forming a semiconductor device structure comprising:  
2                 forming a conductive first plate on a substrate;  
3                 growing at least one nanotube extending substantially vertically from the first  
4         plate that is electrically coupled with the first plate;  
5                 covering the at least one nanotube and the first plate with a dielectric layer;  
6         and  
7                 forming a second plate overlying said first plate that is electrically insulated by  
8         the dielectric layer from the at least one nanotube and the first plate.

1        30.     The method of claim 29 wherein said at least one nanotube has a conducting  
2         molecular structure.

1        31.     The method of claim 29 wherein said at least one nanotube has a  
2         semiconducting molecular structure.

1        32.     The method of claim 29 wherein covering the at least one nanotube and the  
2         first plate comprises:  
3                 encasing the at least one nanotube inside the dielectric layer.